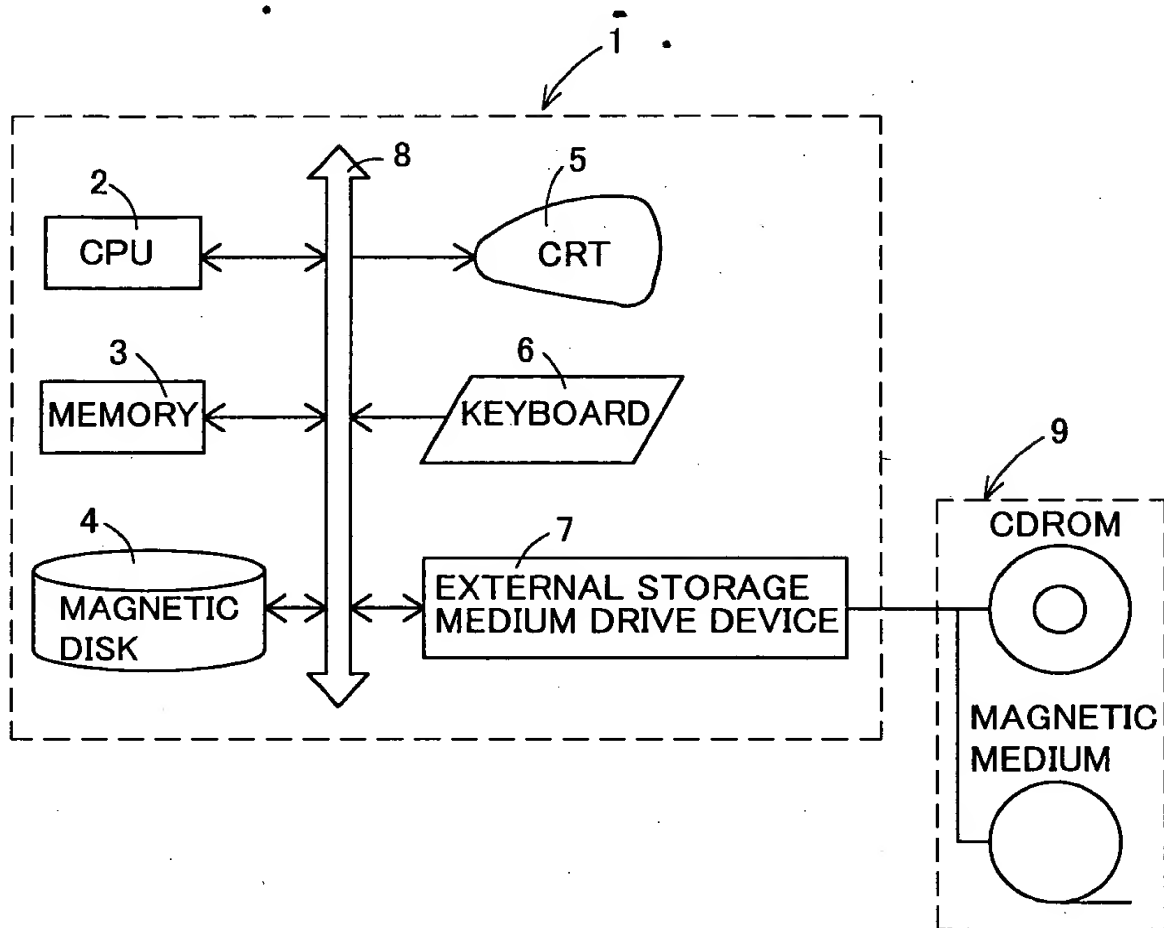


# FIG. 1

STRUCTURAL VIEW OF A WIRING DEVICE IN ONE EMBODIMENT



COPIES TO BE MADE

## FIG. 2

PLAN VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN THE EMBODIMENT

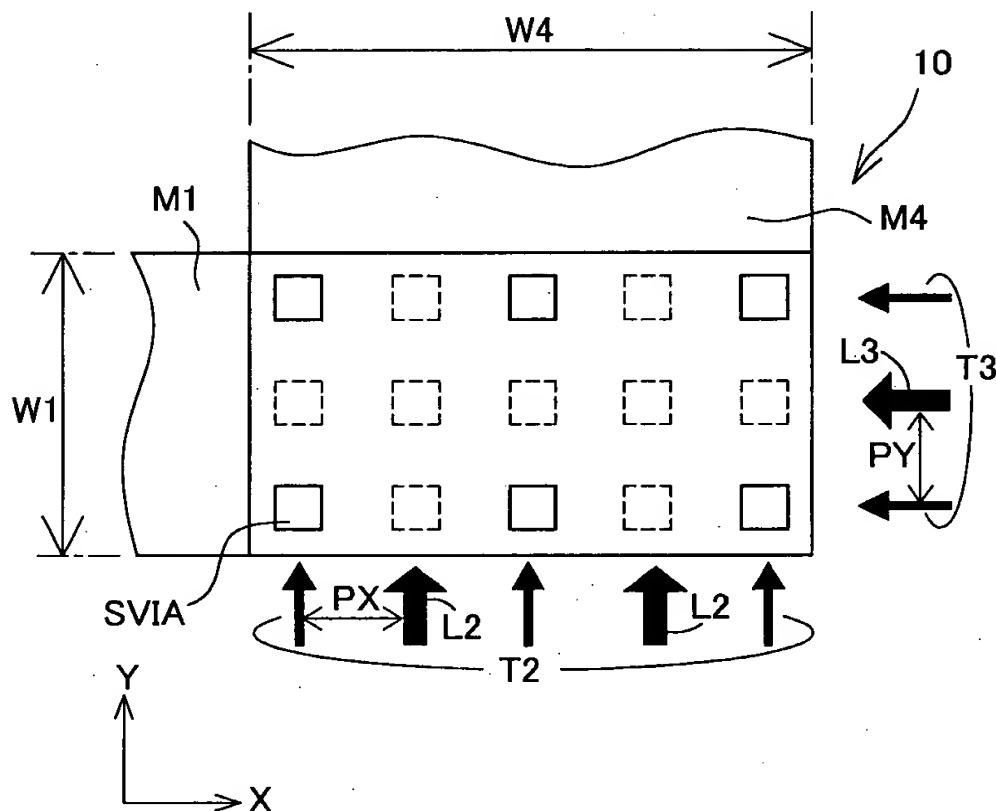
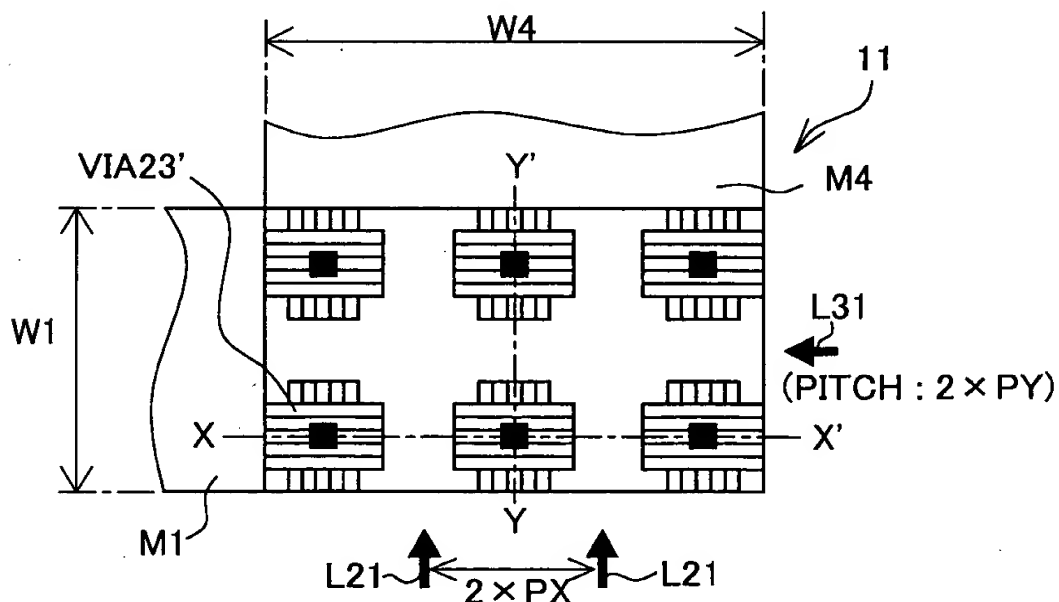
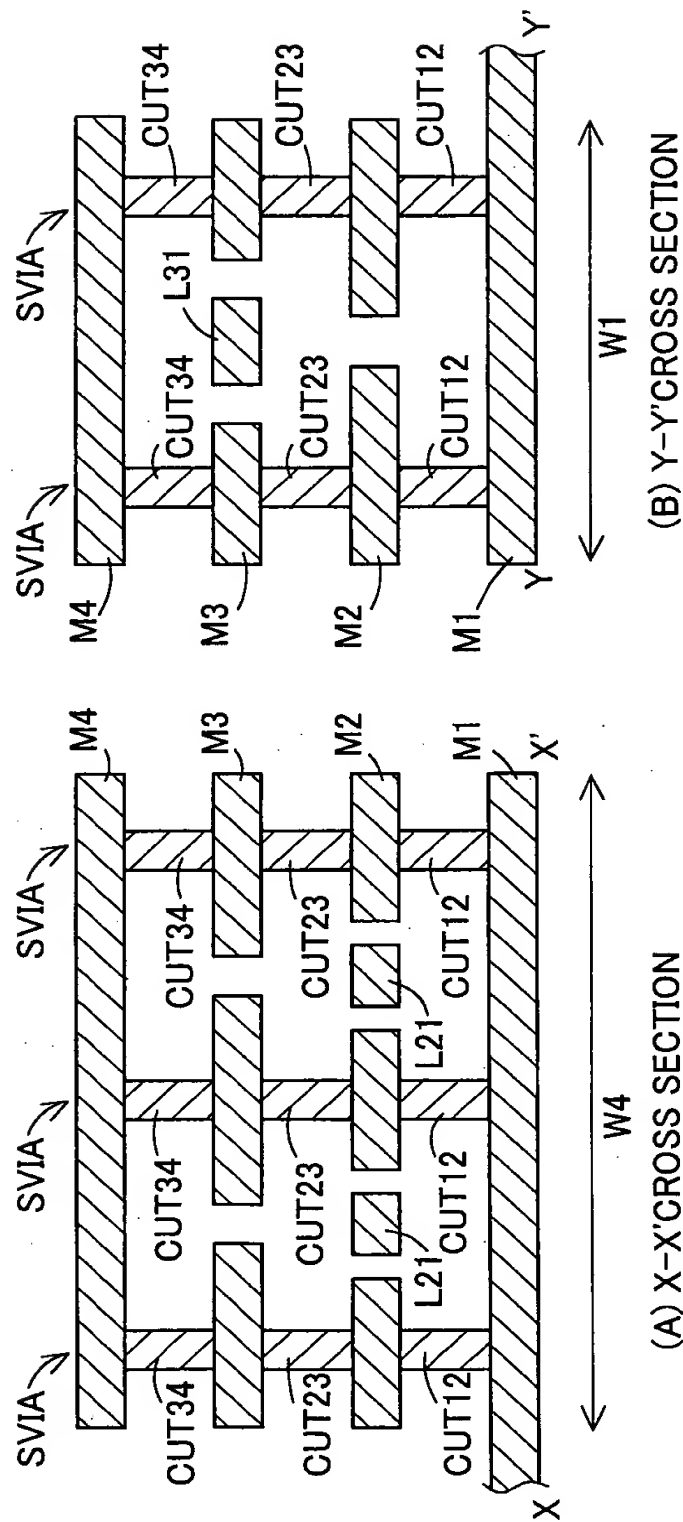


FIG. 2

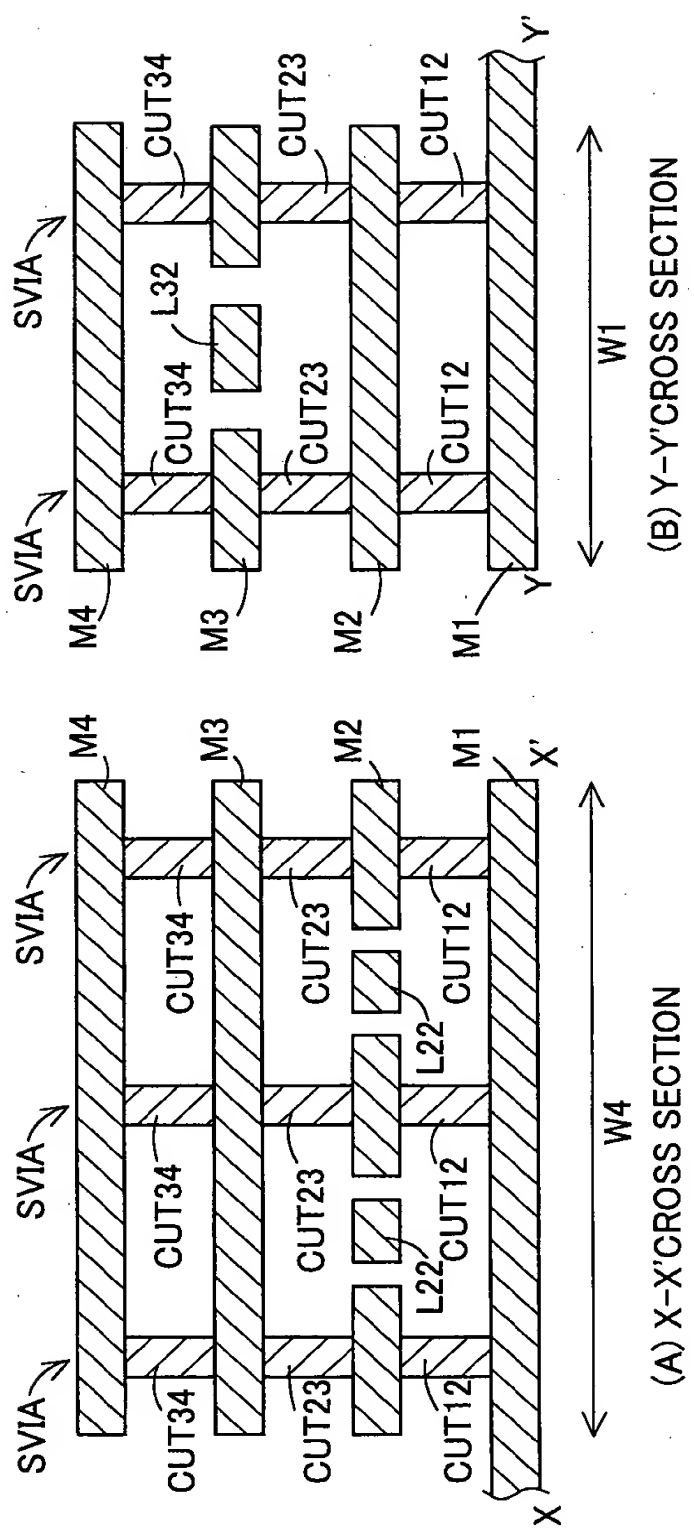


**FIG. 5** CROSS-SECTIONAL VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN THE FIRST SPECIFIC EXAMPLE OF THE EMBODIMENT



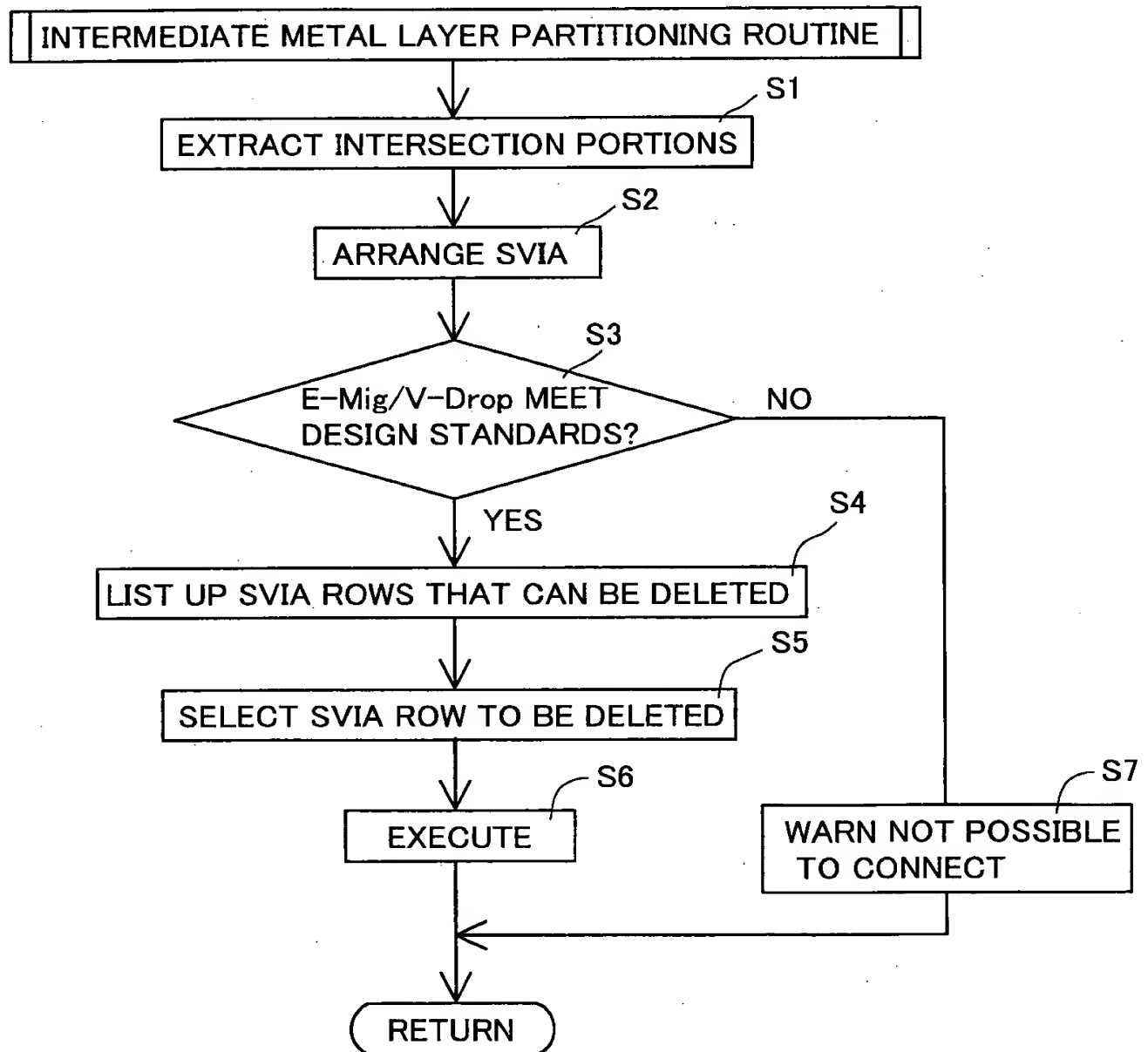
[illegible]

**FIG. 7** CROSS-SECTIONAL VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN THE SECOND SPECIFIC EXAMPLE OF THE EMBODIMENT



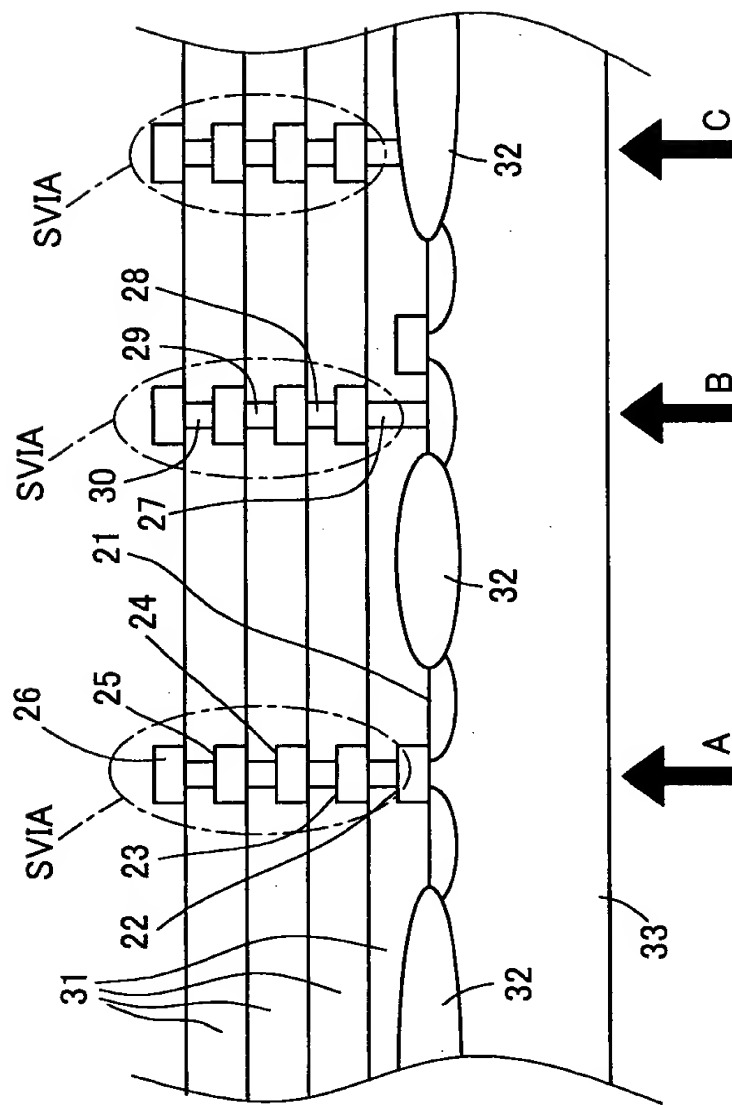
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FLOW CHART SHOWING A WIRING METHOD FOR AN INTERMEDIATE METAL LAYER PARTITIONING ROUTINE IN THE EMBODIMENT



TOP SHEET OF 10

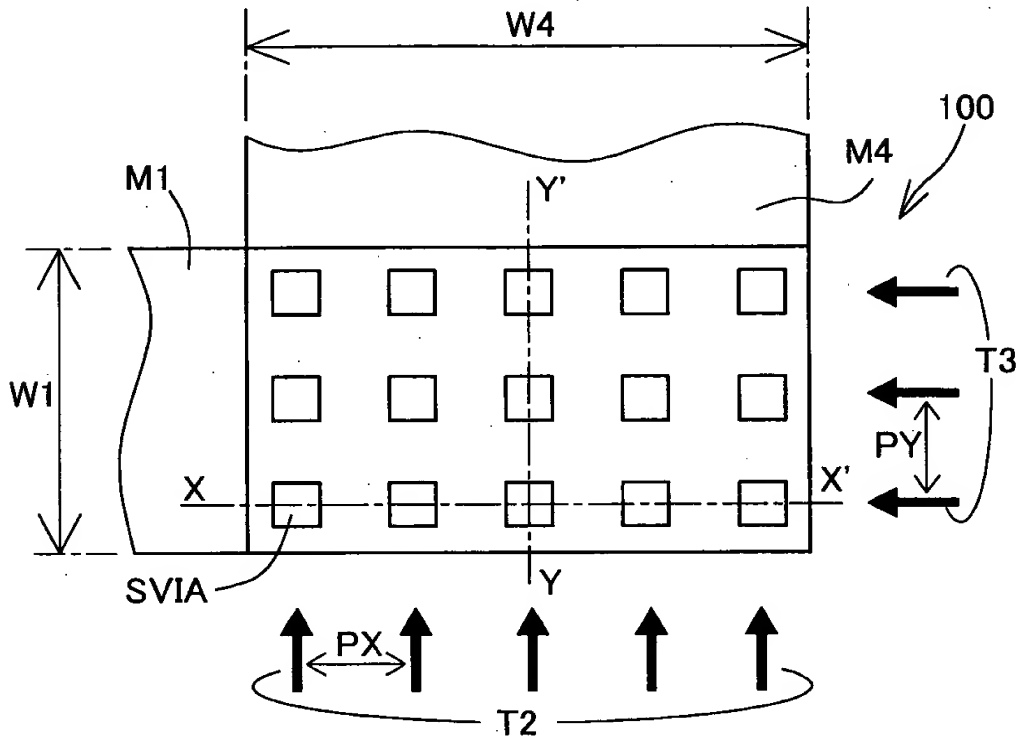
**FIG. 9** CROSS-SECTIONAL VIEW OF A SEMICONDUCTOR DEVICE HAVING A MULTIPLE LAYER WIRING STRUCTURE





# FIG. 10 PRIOR ART

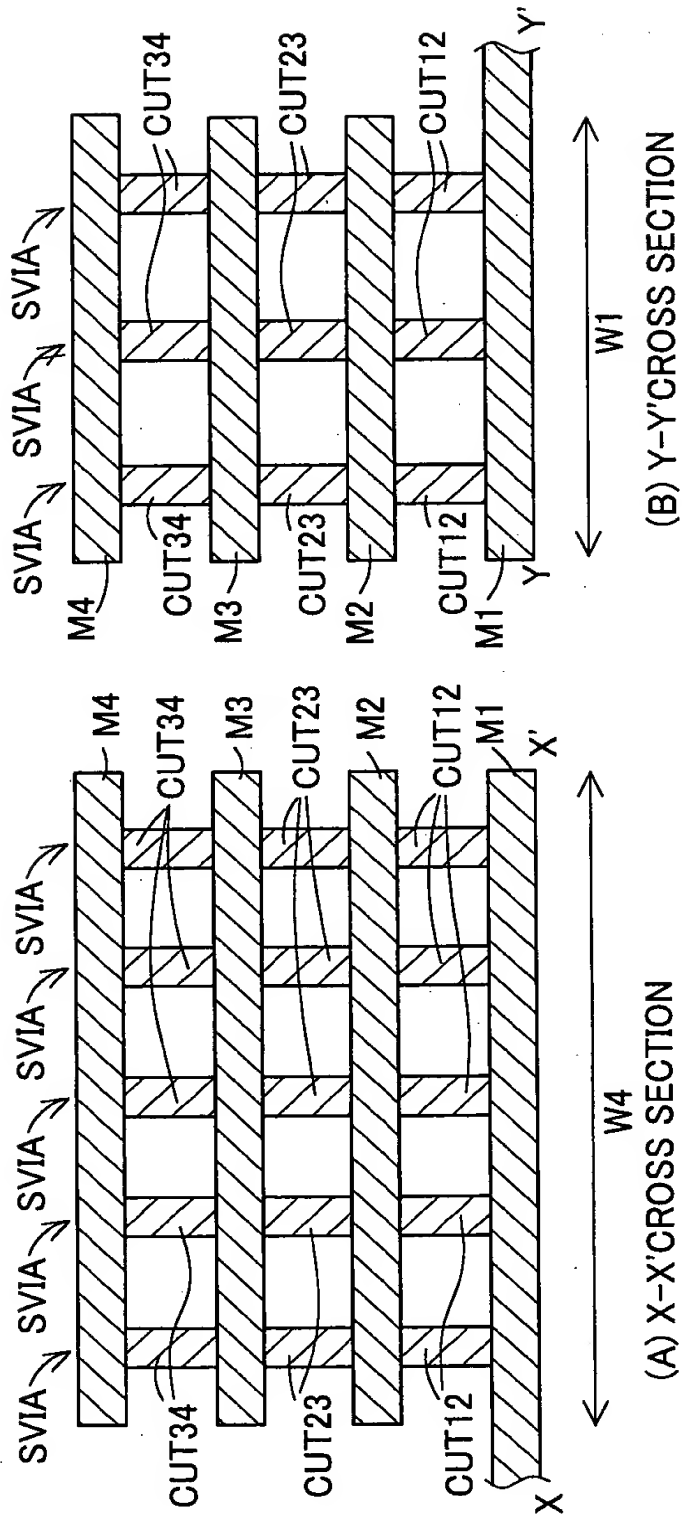
PLAN VIEW SHOWING A CONNECTION BETWEEN METAL WIRING LAYERS IN CONVENTIONAL TECHNOLOGY



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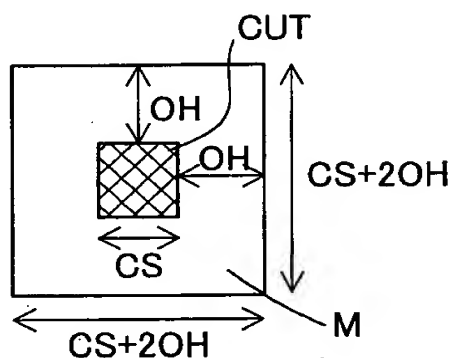
# FIG. 11 PRIOR ART

CROSS-SECTIONAL VIEW SHOWING A CONNECTION BETWEEN METAL  
WIRING LAYERS IN CONVENTIONAL TECHNOLOGY



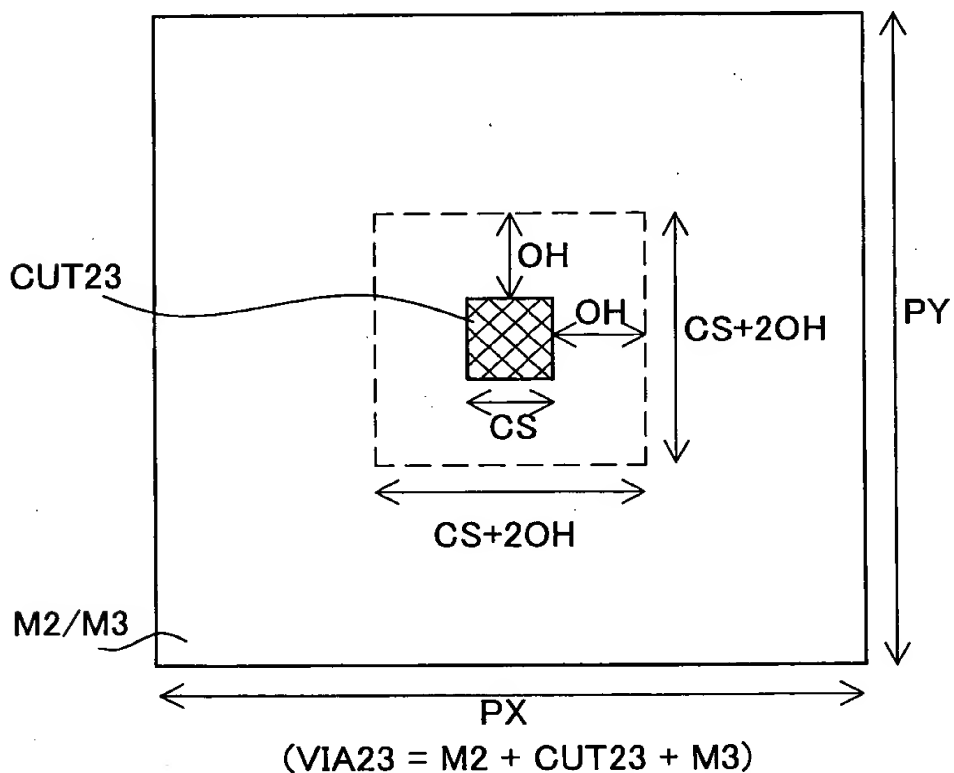
# FIG. 12 PRIOR ART

VIEW OF A BASIC MINIMUM PATTERN OF A VIA



# FIG. 13 PRIOR ART

PATTERN VIEW SHOWING AN INTERMEDIATE LAYER VIA IN CONVENTIONAL TECHNOLOGY



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